



Augmented Sidewall Topology Simulation of Semiconductor Die

Rennier Rodriguez^{1*}, Frederick Ray Gomez¹ and Edwin Graycochea Jr.¹

¹New Product Development and Introduction, STM microelectronics, Inc., Calamba City, Laguna, 4027, Philippines.

Authors' contributions

This work was carried out in collaboration amongst the authors. All authors read, reviewed, and approved the final manuscript.

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ABSTRACT

The paper presents a modified design for wafer level semiconductor devices, using a CAD (computer-aided design) tool for visualization. The discussion provides a specialized manufacturing flow for the augmented die design through advanced wafer fabrication method and wafer cutting technique. Ultimately, the new package design would result for better visual inspection and interface anchoring between the device and the external board.

Keywords: Redistribution layer; sidewall design; silicon die; wafer level.

1. INTRODUCTION

The solderable sidewall or the integration of a recess on the sidewall of a unit to enable a visible formation of solder fillet is becoming a necessity in the construction of any automotive-qualified devices. This improvement in packaging allows automatic optical inspection (AOI) during the placement of surface mount devices on the

external printed circuit board (PCB). The visibility of the of solder fillet is detected by the AOI machine which presence of solder fillet is correlated to good mounting condition and its absence is identified as rejected during surface mount device placement.

The requirement of solderable sidewall is currently established on quad-flat no-leads

*Corresponding author: Email: rennier.rodriguez@st.com;

(QFN) package wherein a segmented mechanical cutting is performed to produce a stepping cut on the sidewall. The sidewall then will be plated with Tin (Sn) to create good formation of solder fillet on the junction since Sn is known to produce good solderability. On the other hand, the conventional design of QFN, the sidewall is composed of bare Copper (Cu) which has poor solderability and does not create solder fillet during unit mounting.

Some products such as Wafer Level Chip Scale Package (WLCSP) has its limitation in terms of AOI readiness due its existing design and construction. Works and studies related to inspection and pattern recognition system and wafer monitoring are shared in [1-5]. The location of solder balls is concealed from optical inspection, as shown in Fig. 1.

As the package becoming smaller, automatic inspection then are becoming a must during detection. In anticipation for automatic inspection, the design of conventional chip-scale packages can be modified through redirecting the redistribution layers (RDL) to the metallized recess formed on the sidewall of the device. This will create a visible solder fillet for AOI during the solder mounting. In this paper, the method and

design in creating a WLCSP product with sidewall interconnects is discussed and presented.

2. PACKAGE DESIGN AND PROCESS IMPROVEMENT

Wafer level packaging became known to some extent due to the continuous reduction of packaging size for surface mount devices. In this case, the resulting wafer level package has the same or very near the size of the Silicon (Si) die to maximize spaces and clearances. This is done through the application of RDL that attaches the bonding pad to the solder balls and layers of dielectric layers to isolate the RDL from electrically active components.

The proposed modification of the design simulated in CAD tool shown in Fig. 2 relocates the solder ball opening that is usually located in the die center to the sidewall of the unit. The recess must be formed first afterwards it is plated with metallic layer wherein solder balls can be attached. The recess that is formed on the sidewall is the portion that will be attached to the PCB during mounting of the unit.

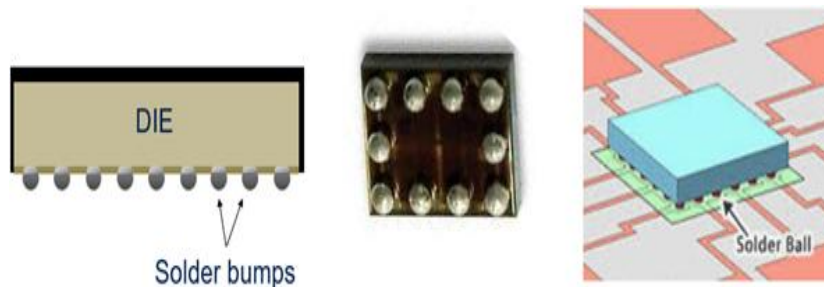


Fig. 1. Solder bumps on wafer level semiconductor device

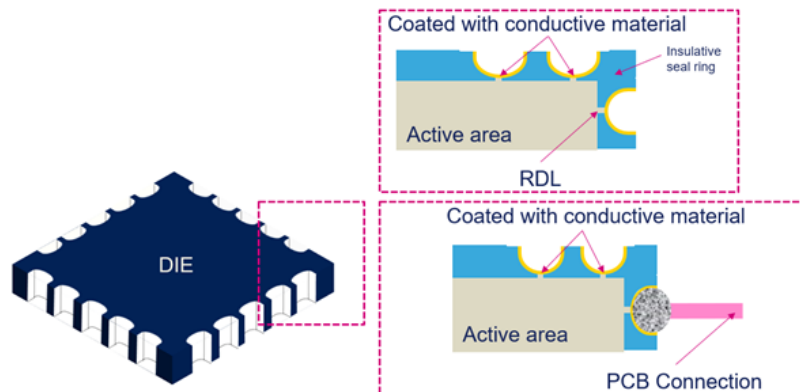


Fig. 2. Augmented design of Silicon die

The recess is isolated from the active through the insulative seal ring. Normally, it is made-up of bare Silicon material. The non-conductive material eliminates the direct contact of the solder or sintered glue to the active portion that may result to electrical shorting or damage.

The Silicon die is normally produced through series of etching, masking, and deposition. A cross-sectional representation of the die is shown in Fig. 3. A passivation layer isolates and protects the active component on the silicon wafer from external contamination during wafer fabrication. A dielectric layer is formed on top of the passivation layer in preparation for the RDL. The dielectric layer 1 produces the layout before the deposition of RDL metallic then at the same time will isolate and limit the interference from the RDL to re-entering the passivation.

The RDL connects the bonding pad to the recess then a dielectric layer 2 is incorporated on top of the RDL. The sidewall topology is formed through plasma etching process then a metallic

coating such Nickel-Aluminum-Gold (Ni-Al-Au) is incorporated to the recess.

Fig. 4 illustrates the method of fabricating the proposed design. The incoming wafer is coated with dielectric layer through deposition process. This process covers the active portion of the silicon wafer excluding the bonding pad. A pattern will be engraved on the edges or the sawing street of the die. This process removes the metal component and will create the define location of the recess. Plasma process will then be performed on the units. The plasma process would etch only the exposed silicon produced by the laser engraving. To produce a suitable recess formation, a depth of 50 – 60% of the total silicon thickness is recommended. Metal is then deposited on the recess portion. RDL is fabricated on top of the dielectric layer 1 and it will be connected to the recess. A dielectric layer 2 is propagated on top of the RDL to isolate the material from external damages.

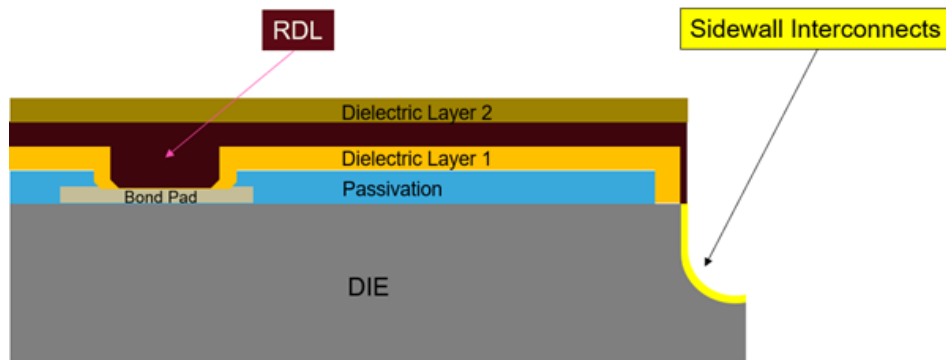


Fig. 3. Cross-sectional stackup view

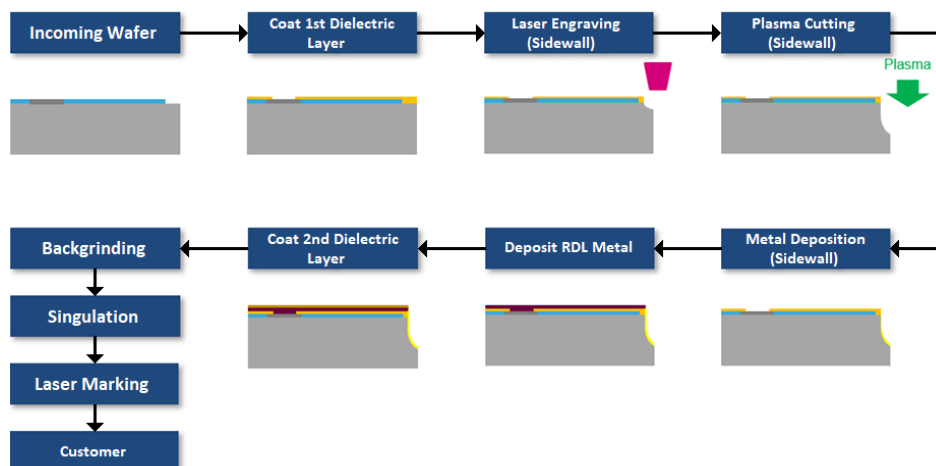


Fig. 4. Wafer fabrication flow

3. CONCLUSION AND RECOMMENDATIONS

The paper discussed an augmented semiconductor die design with a specialized metallized sidewall and the corresponding wafer fabrication process. An advantage of the augmented design is that the solder formation will be visible on the sidewall of the unit, allowing the AOI for the unit. The design includes additional anchoring design between the unit and the PCB. More importantly, the augmented design offers readiness for automotive qualification. Still, prototypes are helpful for future works and are needed to validate the effectiveness of the new semiconductor die. Moreover, quantitative analysis and comparison of visual and thermal inspection, as well as comparison with other fabrications are recommended for expanded discussions.

Though the paper focused on advancement in the semiconductor die design, continuous design and process improvement is essential to realize technology development and at the same time achieve high quality performance of semiconductor products and its assembly manufacturing. Works and ideas shared in [6-10] are valuable on this purpose.

DISCLAIMER

The products used for this research are commonly and predominantly used products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Dave N, et al. PCB defect detection using image processing and embedded system. *International Research Journal of Engineering and Technology*. 2016;3(5);1897-1901.
2. Oh HW, et al. Gerber-character recognition system of auto-teaching program for PCB assembly machines. *SICE 2004 Annual Conference*. Japan. 2004;1;300-305.
3. Lee H, et al. A deep learning model for robust wafer fault monitoring with sensor measurement noise. *IEEE Transactions on Semiconductor Manufacturing*. 2017;30(1);23-31.
4. Kim HT, et al. Automatic focus control for assembly alignment in a lens module process. *2009 IEEE International Symposium on Assembly and Manufacturing*. South Korea. 2009;292-297.
5. Freed M, et al. Autonomous on-wafer sensors for process modeling, diagnosis, and control. *IEEE Transactions on Semiconductor Manufacturing*. 2001;14(3);255-264.
6. Rodriguez R, et al. Semiconductor package design solution for addressing high-density configuration. *Journal of Engineering Research and Reports*. 2020;16(3);1-6.
7. Saha S. Emerging business trends in the semiconductor industry. *Proceedings of PICMET '13: Technology Management in the IT-Driven Services (PICMET)*. USA. 2013;2744-2748.
8. Gomez FR, Seguido R. Improvement on semiconductor substrate design with package modeling and simulation for mitigation of delamination and voids. *Journal of Engineering Research and Reports*. 2018;2(4);1-9.
9. Yeap LL. Meeting the assembly challenges in new semiconductor packaging trend. *34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT)*. Malaysia. 2010;1-5.
10. Sumagpang Jr. A, et al. Introduction of reverse pyramid configuration with

package construction characterization for die tilt resolution of highly sensitive multi-stacked dice sensor device. 22nd IEEE

Electronics Packaging Technology Conference (EPTC). Singapore. 2020;140-146.

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